Terahertz chiral edge states enable inner-chip state transition and interchip communications over wireless terminals

Hong Chen (陈 红)^{1†}, Hang Ren (任 航)^{1†}, Wenya Wang (王文雅)¹, Zhaohua Xu (许兆华)¹, Yanfeng Li (栗岩锋)², Quan Xu (许 全)², Jiaguang Han (韩家广)², and Su Xu (徐速)^{1*}

¹State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun 130012, China

²Center for Terahertz Waves and College of Precision Instrument and Optoelectronics Engineering, Key Laboratory of Optoelectronic Information Technology (Ministry of Education), Tianjin University, Tianjin 300072, China

S1. The edge dispersions tuned by on-site edge potentials

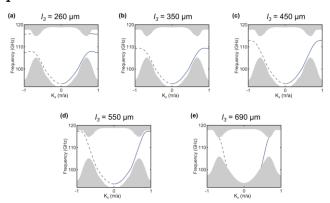


Fig. S1. The dispersion diagrams of CESs controlled by the side length of the outmost air holes. (a)-(e) Band structures with the side length of the outmost air holes I_3 = 260, 350, 450, 550, and 690 μ m. The blue lines and the gray regions represent the edge dispersion and the projected bulk dispersion, respectively. The solid and dashed blue lines indicate opposite valleys.

The linear dispersion relationships of CESs can be obtained by tuning the on-site edge potentials. For this work, adjusting the side length of the outmost air holes is one approach to tuning the on-site potentials. In Figs. S1(a)-S1(e), we displayed the band structures of the CESs with steadily increasing side lengths of the outmost air holes for $I_3 = 260$, 350, 450, 550 and 690 µm. It can be observed that the group velocity of CESs within the bandgap continuously changes with the increase of *l*₃ and the dispersion curves of CESs bend upward as *l*³ increases. To achieve stable transmission, minimize dispersion effects and cover the entire bandgap width, we adjust the side length of the outermost air holes to $l_3 = 550 \mu m$ to attain the linear group velocity. Consequently, our work

focuses on $\it l_3$ = 550 μm , where the CESs exhibit linear dispersion curves at K and K' valleys.

S2. The minimal impact of the PP film on wireless interconnection system

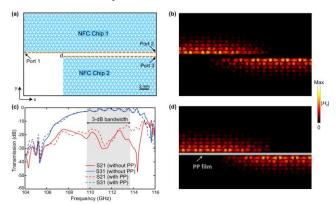


Fig. S2. Topological wireless energy transfer system with and without the PP film. (a) The schematic illustration of the inter-chip energy transfer system. The VPC-air boundaries of the NFC Chip 1 and NFC Chip 2 are aligned and separated by d=0.7 mm. The orange dashed lines mark the VPC-air interface. Port 1 is the exciting end of electromagnetic signals and Port 2 and Port 3 are the receiving ends. (b) The $|H_z|$ field distribution of the system at 110 GHz when Port 1 is excited. (c) The Sparameters of the systems in (b) and (d). The shaded area represents the 3-dB bandwidth with NFC chip transmitted efficiency higher 50%. (d) The $|H_z|$ field distribution of the system at 110 GHz when a PP film is added between the chips.

A fantasy of the wireless interconnection system between mobile phones based on NFC chips is made in Fig. 5. Considering the phone packaging and fixation aspects, a PP film is added between the chips. To confirm whether the PP film has a significant impact on wireless transmission, we

[†]These authors contributed equally to this work.

^{*}Corresponding author: xusu@jlu.edu.cn

discussed the energy transfer situations both with and without the PP film between the chips. The schematic view of the topological wireless energy transfer system is shown in Fig. S2(a), where the VPC-air boundaries of the two NFC chips are aligned and separated by a distance of d = 0.7 mm. When the Port 1 of NFC Chip 1 is excited, the $|H_z|$ field distributions at 110 GHz without and with the PP film between the chips are shown in Figs. S2(b) and S2(d), respectively, both demonstrating excellent wireless energy transmission capabilities. To quantitatively assess the impact of the PP film on wireless energy transmission, we have plotted the transmission curves of the chips for both scenarios, as shown in Fig. S2(c). The scattering parameters in Fig. S2(c) show a high level of energy transfer efficiency and isolation, whether it has PP films or not, indicating the minimal impact of the PP film on wireless energy transfer.

S3. The frequency scalability of the chip

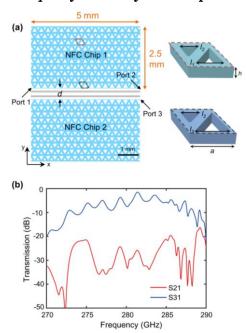


Fig. S3. The frequency scalability of the NFC chips. (a) The schematic illustration of the wireless interconnection system working at around 280 GHz. (b) The S-parameters of the system working at around 280 GHz.

Our NFC chip could work at higher frequencies by shrinking its size. As shown in Fig. S3(a), the size of the unit is reduced to achieve the working frequency at around 280 GHz, the lattice constant $a=300~\mu m$, thickness $h=200~\mu m$, separation distance d=0.24~mm, side lengths of the air hole $I_1=I_0+\Delta I$, $I_2=I_0-\Delta I$, with $I_0=150~\mu m$, $\Delta I=a/8$, $I_3=225~\mu m$. The simulation transmission curves in Fig. S3(b) exhibit a high degree of energy transfer efficiency at around 280 GHz. Actually, the operating frequency of the NFC chips can be

extended to higher frequencies, showing excellent frequency scalability.

S4. Calculation method of transmission efficiency

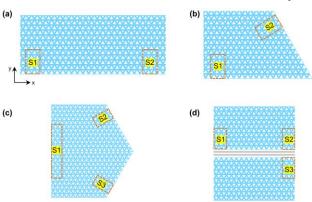


Fig. S4. Approach to calculated transmission efficiency through the ratio of power integrations. (a-d) Calculated integration areas of Figs. 2(f), 4(e), 5(c) and 5(d) and Fig. S2(a) are highlighted by orange dashed rectangles, respectively.

In the full-wave simulation, the silicon tapered pins are added to couple the TE_{10} -mode of the WR-8 metallic rectangular waveguide into the chip. It is worth noting that such coupling conversion is unnecessary in a full VPC chip system. To investigate the realistic transmission loss within the chip, based on full-wave simulation results, we calculated the transmission efficiencies within the chip through the power integral ratio of the areas^[1-2]. The relevant integration areas S1, S2 and S3 of Figs. 2(f), 4(e), 5(c) and 5(d) and Fig. S2(a) are highlighted by orange dashed rectangles in Fig. S4.

S5. The experimental feasibility of the chip

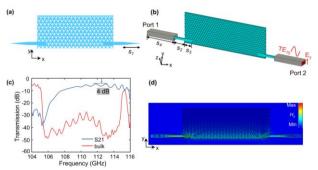


Fig. S5. (a) The full-wave simulation setup of the chip. (a) The schematic view of the chip with two silicon tapered pins. (b) The view of full-wave simulation setup with the WR-8 rectangular metal waveguides and the chip. (c) Transmission curves of the full-wave simulation. (d) The $|H_z|$ field distribution at 110 GHz.

Port-to-Port (WR-8) full-wave simulation, as shown in Fig. S5, is used to illustrate the feasibility of the experiment. Fig. S5(a) shows the schematic view of the chip with two silicon tapered pins. The full-wave simulation setup, containing two WR-8 rectangular metal waveguide ports, is shown in Fig. S5(b). The TE₁₀-

mode electromagnetic wave is coupled to the chip via the tapered pins. The parameters related to the tapered pins are as follows: $s_I=5$ mm, $s_2=3$ mm, $s_3=2.5$ mm, and the length of WR-8 waveguide is $s_4=8$ mm. The transmission curves and the $|H_z|$ field distribution at 110 GHz are depicted in Figs. S5(c) and S5(d), respectively. The highest transmission coefficient S21 is around -4 dB. The material loss of high-resistance silicon ($\varepsilon_{silicon}=11.7$, $\rho=10$ k Ω .cm) is low. The smallest size of the air hole is about 280 µm, which is processable by commercial photolithography technique. Besides, in practical experiments, the vector network analysis system can be used to measure the chip. In all, the port-to-port full-wave simulation results show a certain potential and feasibility of the experiment.

References

- 1. W. Li, Q. Chen, Y. Sun, S. Han, X. Liu, Z. Mei, X. Xu, S. Fan, Z. Qian, H. Chen, and Y. Yang, "Topologically Enabled On-Chip THz Taper-Free Waveguides", Adv. Optical Mater. **11**, 2300764 (2023)
- 2. G. Wei, Z. Liu, H. Wu, L. Wang, S. Wang, and J. Xiao, "Boundary configured chiral edge states in valley topological photonic crystal", Opt. Lett. 47, 3007-3010 (2022).